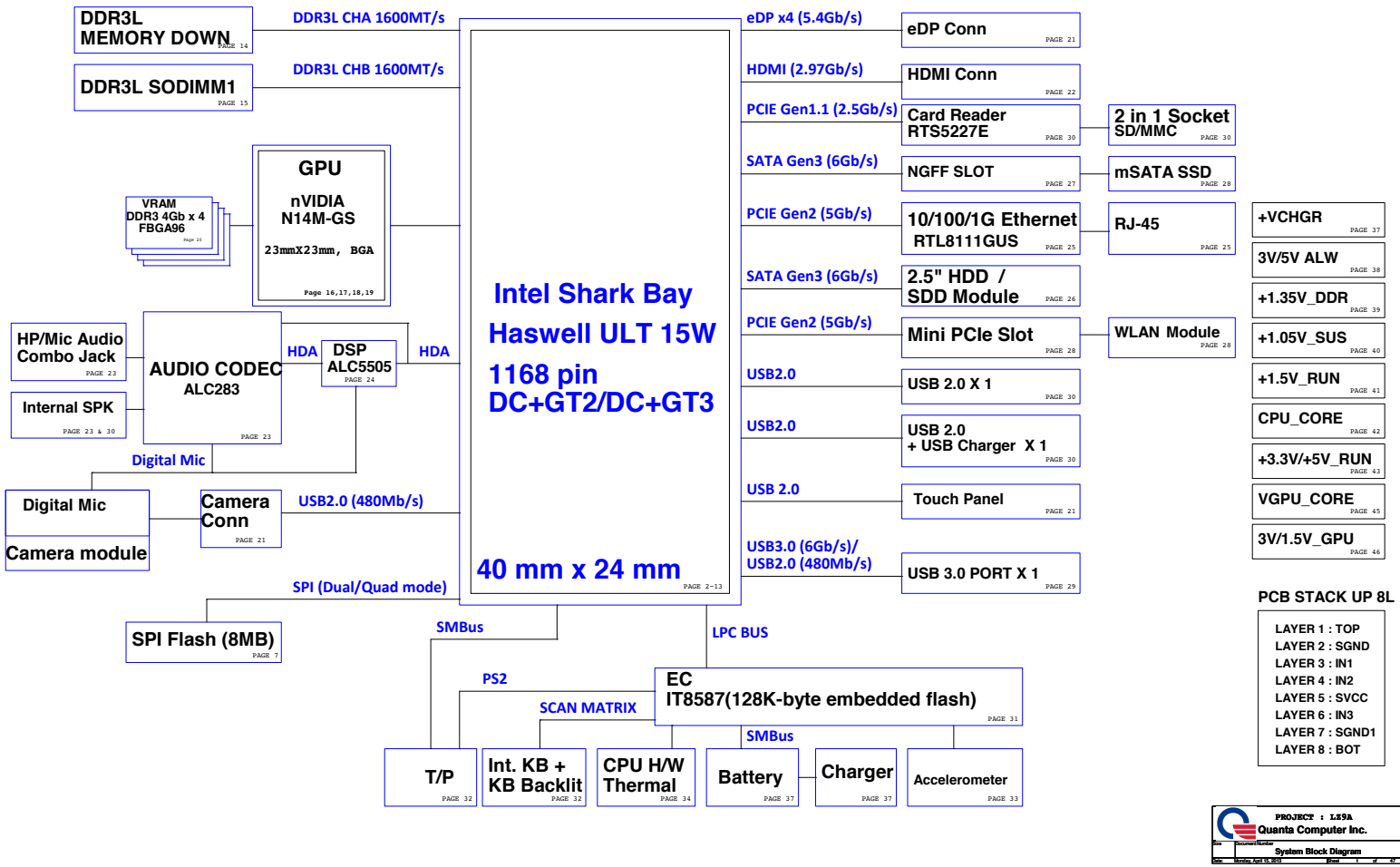


LZ9A 14" OPTIMUS

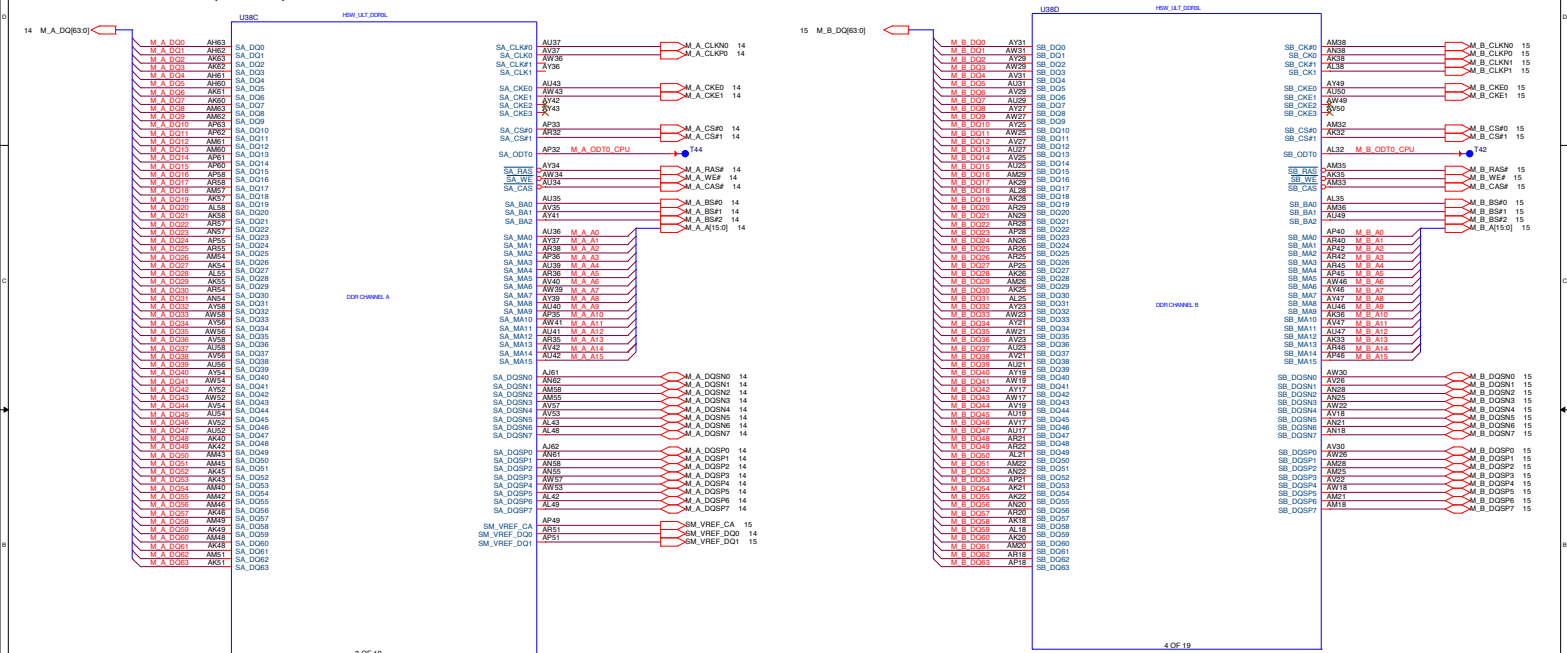
INTEL SHARK BAY ULT ONE CHIP PLATFORM



A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

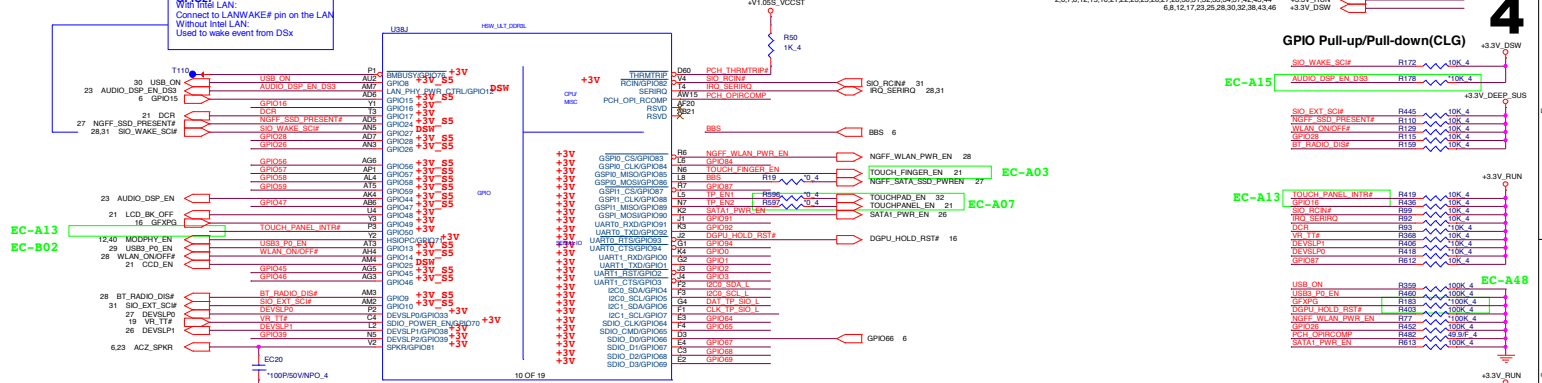


Haswell ULT (DDR3L)



Haswell ULT (GPIO, LPIO, MISC)

GPIO27
With V85 LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from Dsx



Thunderbolt ID **GPIO84**

Supported	0
Not Supported	1



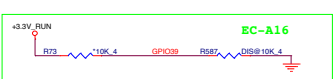
Audio DSP ID **GPIO47**

Supported	0
Not Supported	1



DGPU SELECT **GPIO39**

Supported	0
Not Supported	1



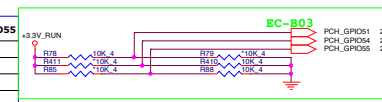
Model ID **GPIO45** **GPIO46**

LZ5-UMA	0	0
LZ9-UMA	0	1
LZ9A-DIS	1	0
LZB	1	1



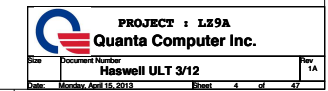
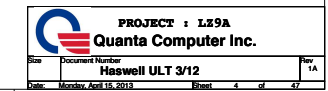
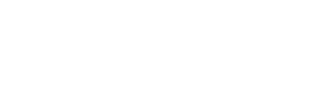
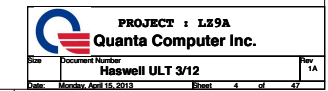
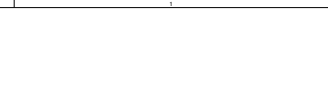
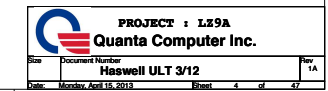
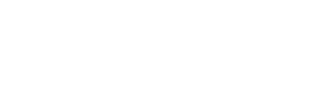
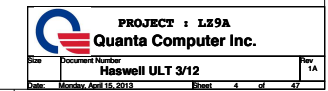
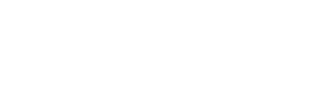
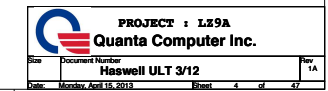
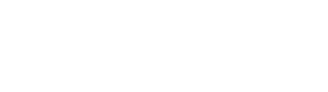
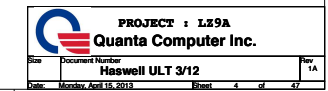
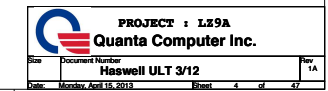
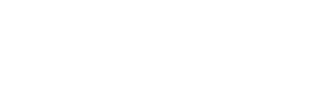
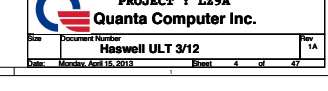
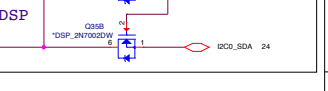
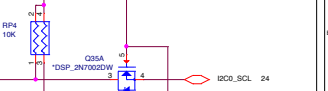
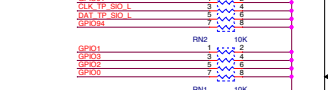
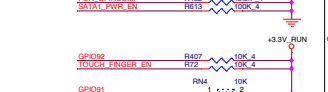
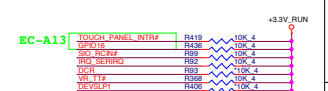
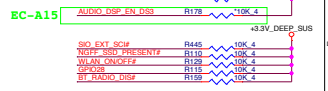
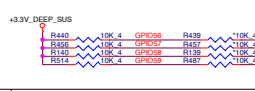
Board ID **GPIO51** **GPIO54** **GPIO55**

SDV	1	1	1
SIV	1	1	0
SIT	1	0	1
SVT	1	0	0

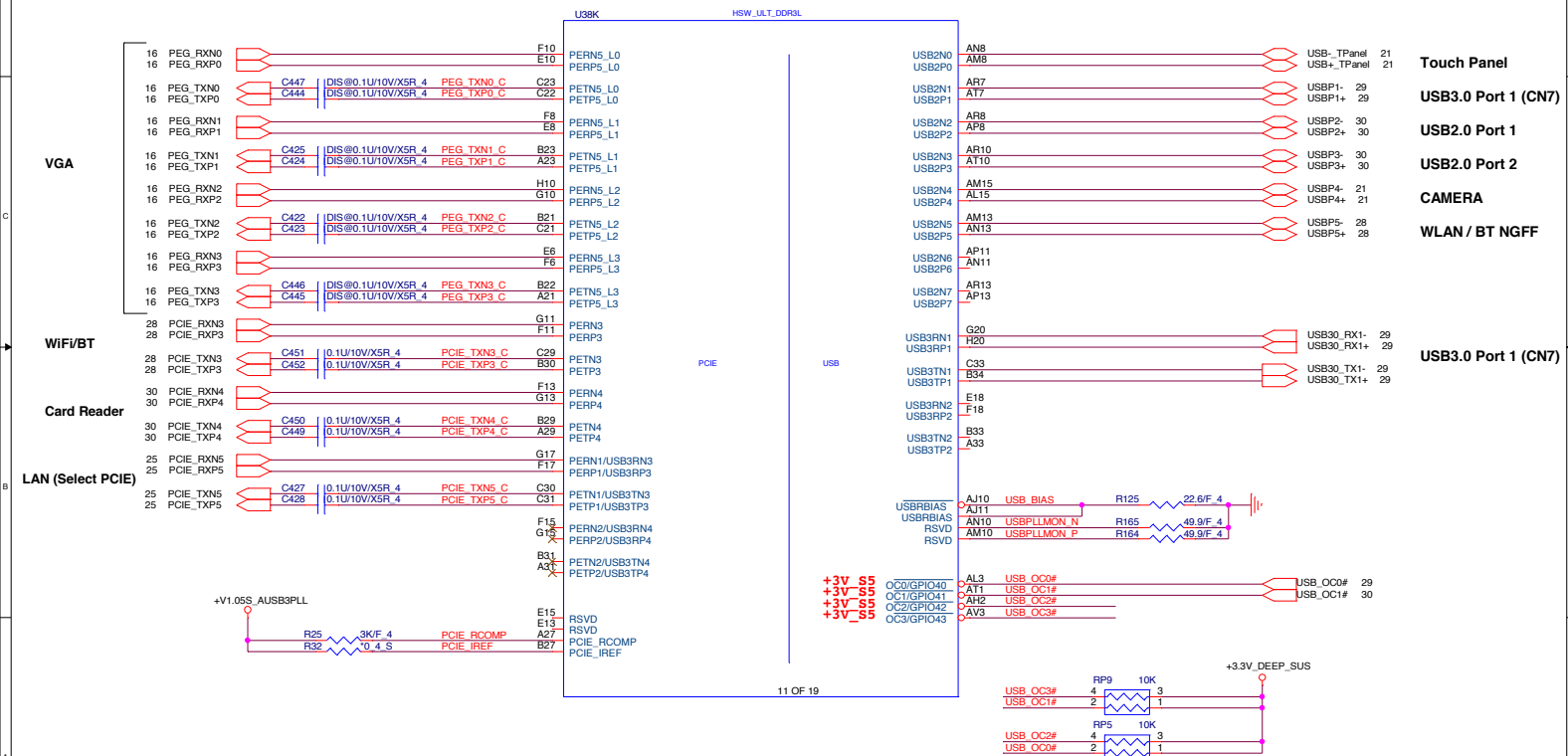


DDR3L Memory Down ID Table

Vendor	Description	Size	Quanta P/N	GPIO[56,57,58,59]
Default				1111
Samsung	K4B8G1646B-MYK0 (B/4Gb/35nm/DDP)	8Gb x 16	AKDSFG6T500	1110
Micron	MT41K512M16YHA-125:E(V80A/4Gb/30nm/DDP)	8Gb x 16	AKDSFG6T100	1101
ELPIDA	EDJ8416E6MB-GN-F(F/4Gb/30nm/DDP)	8Gb x 16	AKDSFG6T402	1100
SK hynix		8Gb x 16		XXXX
Samsung	K4B4G1646B-HYK0(B/4Gb/35nm)	4Gb x 16	AKDSFG6T500	1011
Micron	MT41K256M16HA-125:E(V80A/4Gb/30nm)	4Gb x 16	AKDSJG6T100	1010
ELPIDA	EDJ4216EF6B-PN-F(F/4Gb/30nm)	4Gb x 16	AKDSJG6T403	1001
SK hynix	H5TC46G3AFB-PN-A(D/4Gb/29nm)	4Gb x 16	AKDSJG6T400	1000



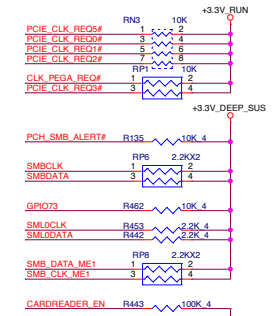
Haswell ULT (PCIE,USB)

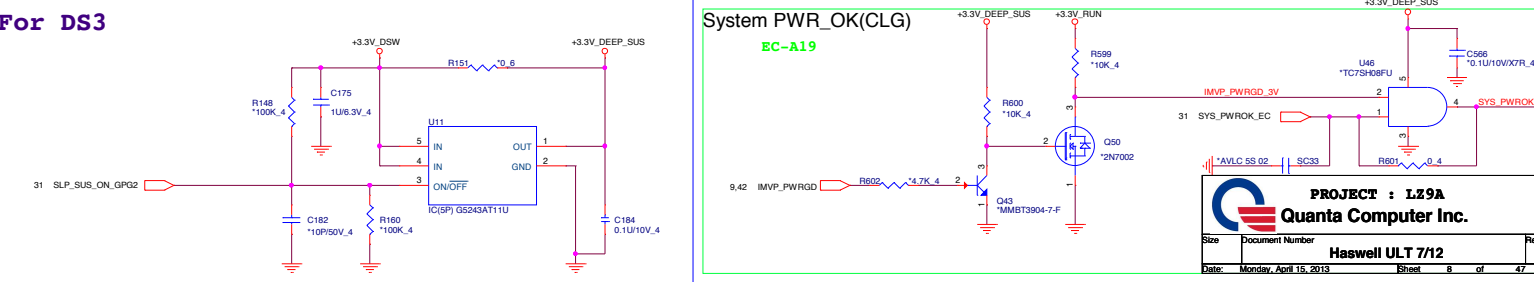


PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 4/12	1A
Date	Monday, April 15, 2013	Sheet 5 of 47



[illegible][illegible]



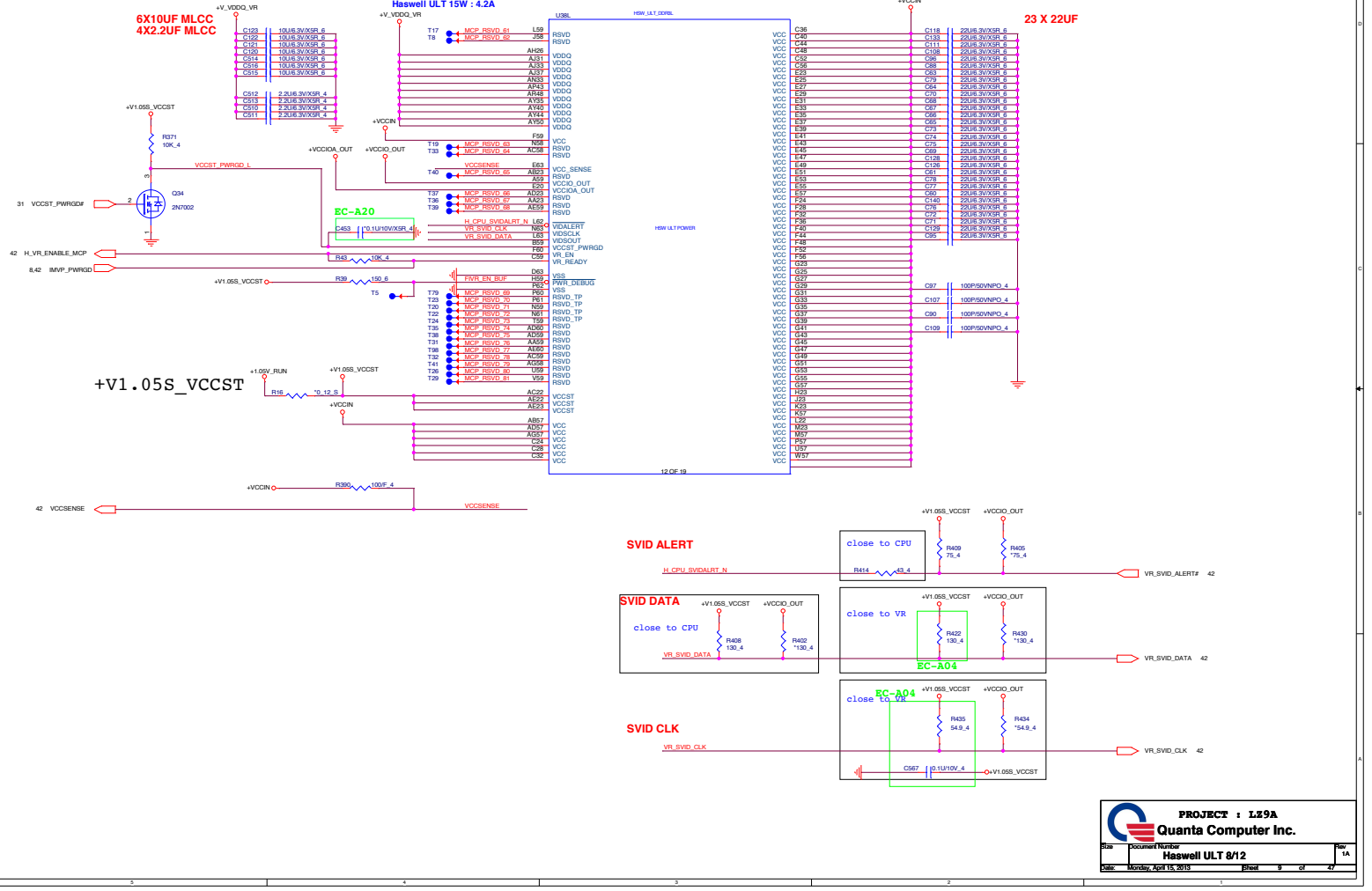
Haswell ULT MCP (POWER)

CPU VCC
Haswell ULT 15W : 32A

CPU VDDQ
Haswell ULT 15W : 4.2A

23 X 22UF

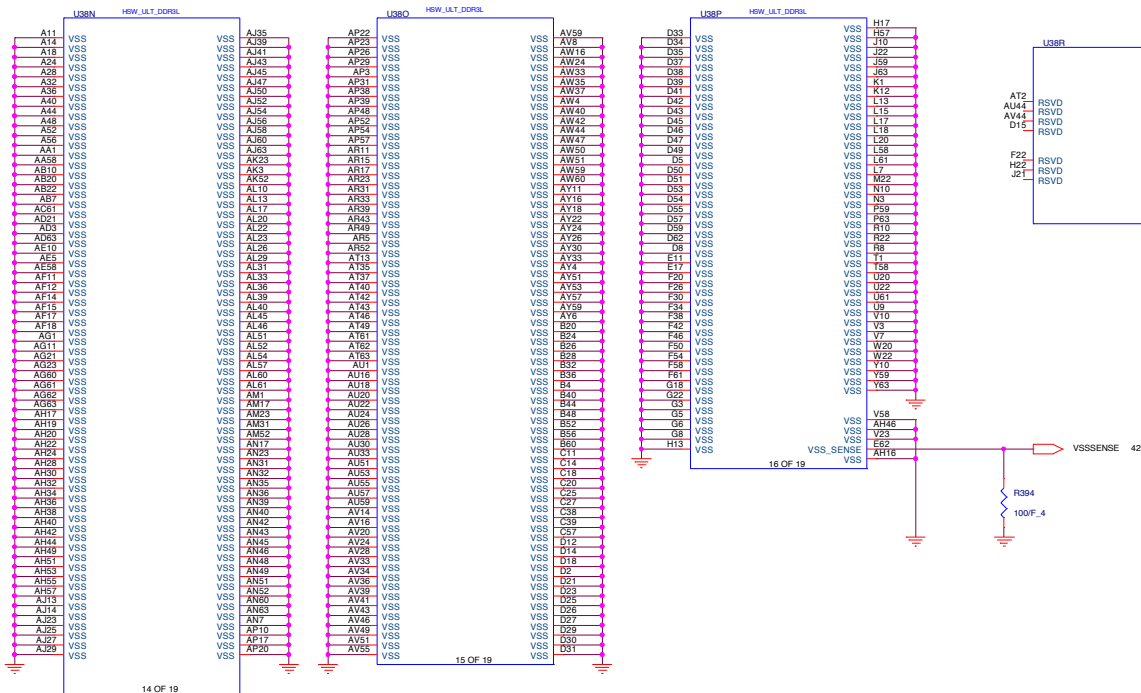
6X10UF MLCC
4X2.2UF MLCC

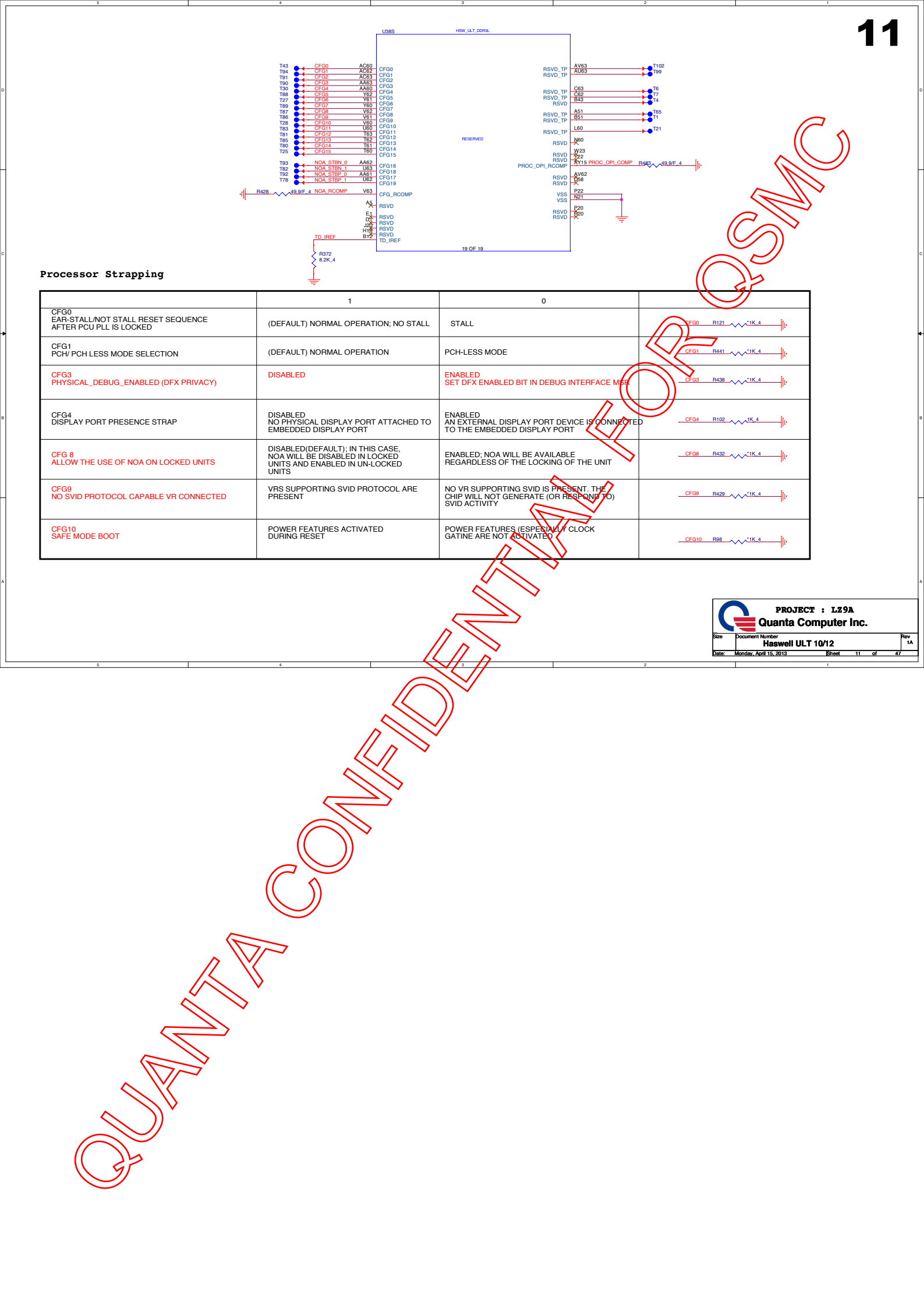


SVID ALERT

SVID DATA

SVID CLK

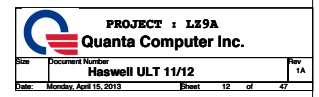
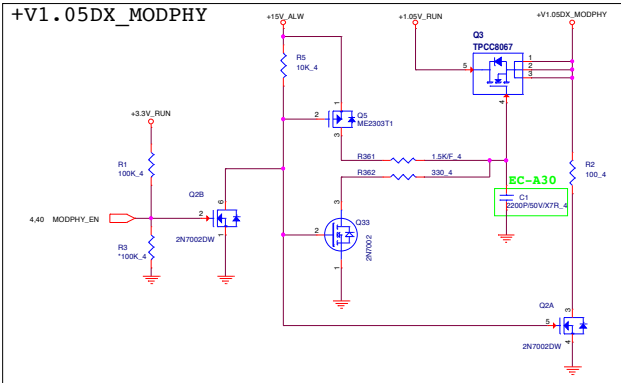


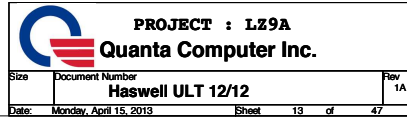


11

11

11







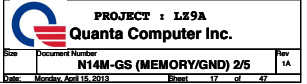




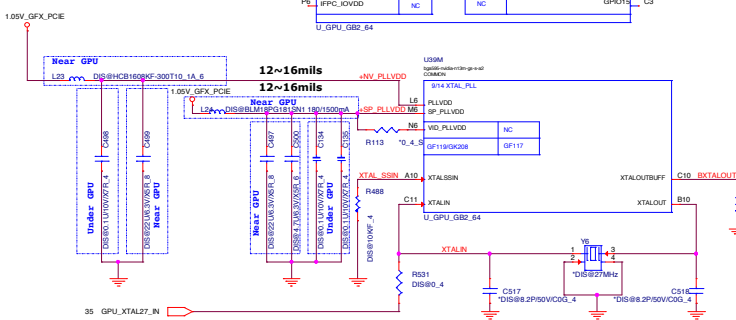
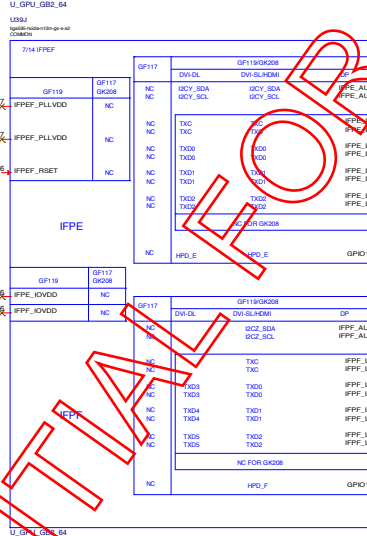
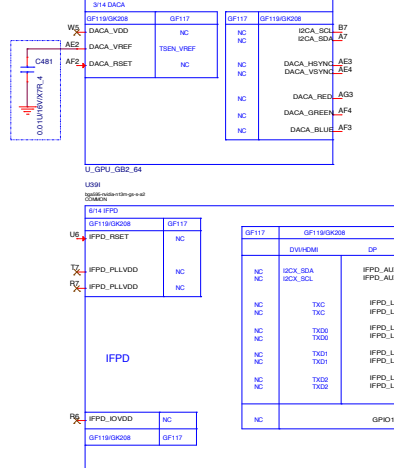
GPU Power Rail	Nominal Value	Comments
HVDD	GPU SKU Specific	GPU Core power rail
FBVDD	1.35 V or 1.5 V	VRAM Core power for Frame Buffer I/O power
FBVDDQ	1.35 V or 1.5 V or 1.8 V	VRAM I/O and GPU Frame Buffer I/O power
FPX_VDDO	1.05 V or 3.3 V	Power/P2 Buckles
FPX_VDD	1.05 V or 3.3 V	Integrated Display Display PLL Power Rails
PEX_VDDIOV	1.05 V or 3.3 V	GPU PCIe interface power rail
PEX_VDDIO_V3, PEX_VDDIO_V3	1.05 V	GPU PCIe PLL Power Rails
FB_VDDIO_V3	1.05 V or 3.3 V	GPU PCIe PLL Power Rails
FB_VDDIO_V3	1.05 V	Frame Buffer PLL
FB_VDDIO_V3 (Q62-44 and Q64-38)	1.05 V	Frame Buffer PLL and DLL Power Rail
FB_VDDIO_V3 (Q62-44 and Q64-38)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLL_VDDIO, CLKPLL_VDDIO, USPLL_VDDIO	1.05 V	Core Clock PLL Analog Power Rail
VDD_PLLVDD	1.05 V	VDDIO Pinct Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DACX_VDDIO	3.3 V	Power the DACs
IOVDDIOV3(V3)	3.3 V	Power slower logic such as GPIOs, I2C, AUX channels and SLI


Notes:

1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the I/F link (see Chapter 8, Digital Displays).
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

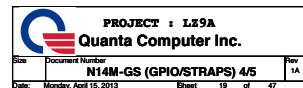


Optimus:
All unstuff , one Cap stuff 10K ohm

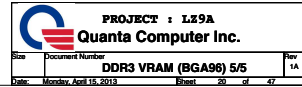


	PROJECT : LZ9A Quanta Computer Inc.		
	N14M-GS (DISPLAY) 3/5		Rev 1A
Size Document Number	Date: Monday April 15, 2019		Sheet 18 of 47

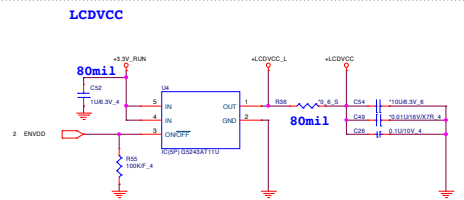
QUANTA CONFIDENTIAL



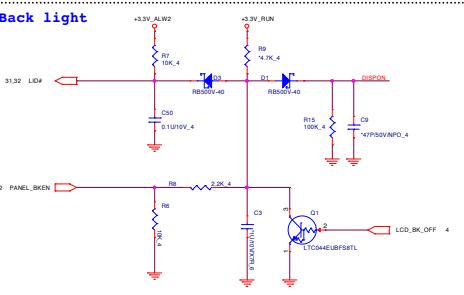
QUANTA CONFIDENTIAL



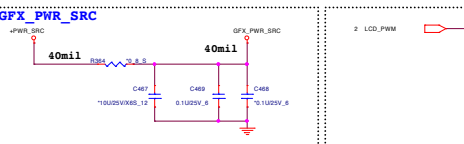
LCDVCC



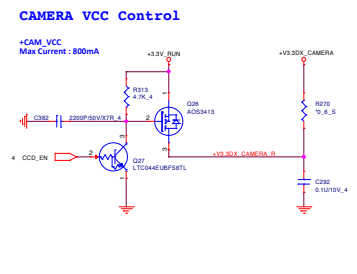
Back light



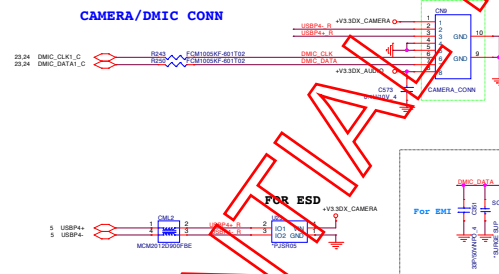
GFX_PWR_SRC



CAMERA VCC Control



CAMERA/DMIC CONN

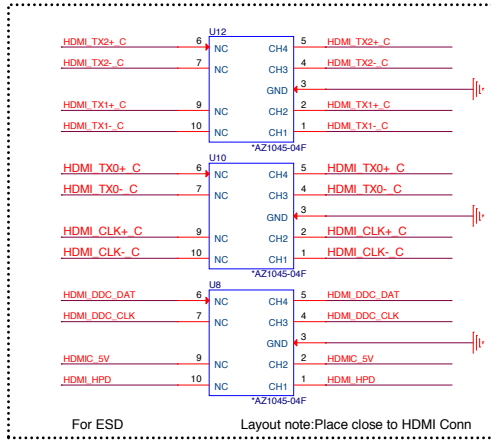
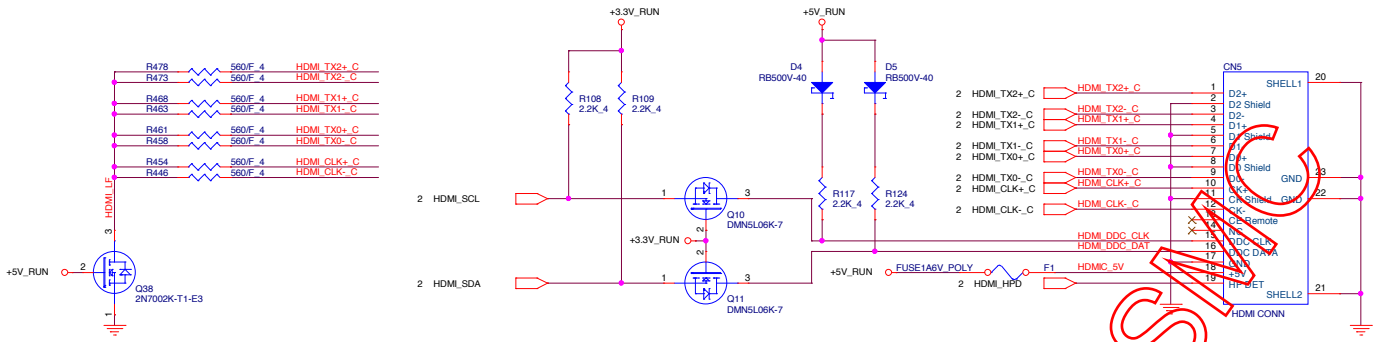


FOR ESD

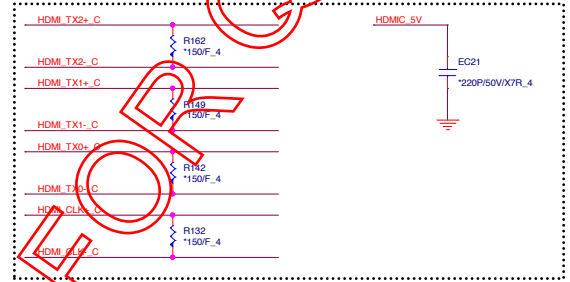
For EMI

PROJECT : L19A	
Quanta Computer Inc.	
Rev	1A
LCD/CAMERA/Touch Panel	
Date	Monday, April 19, 2010
Rev	1

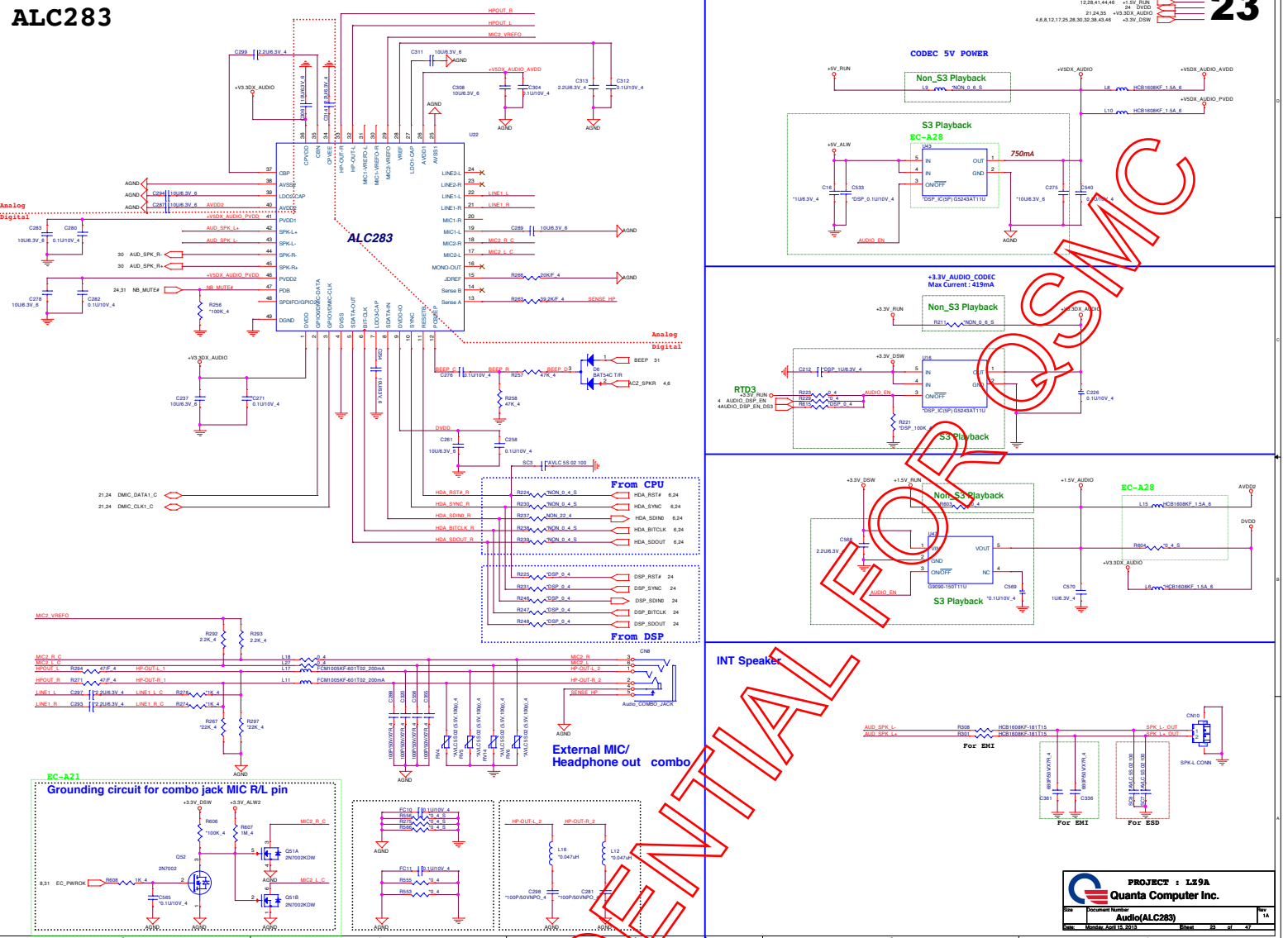
CONFIDENTIAL

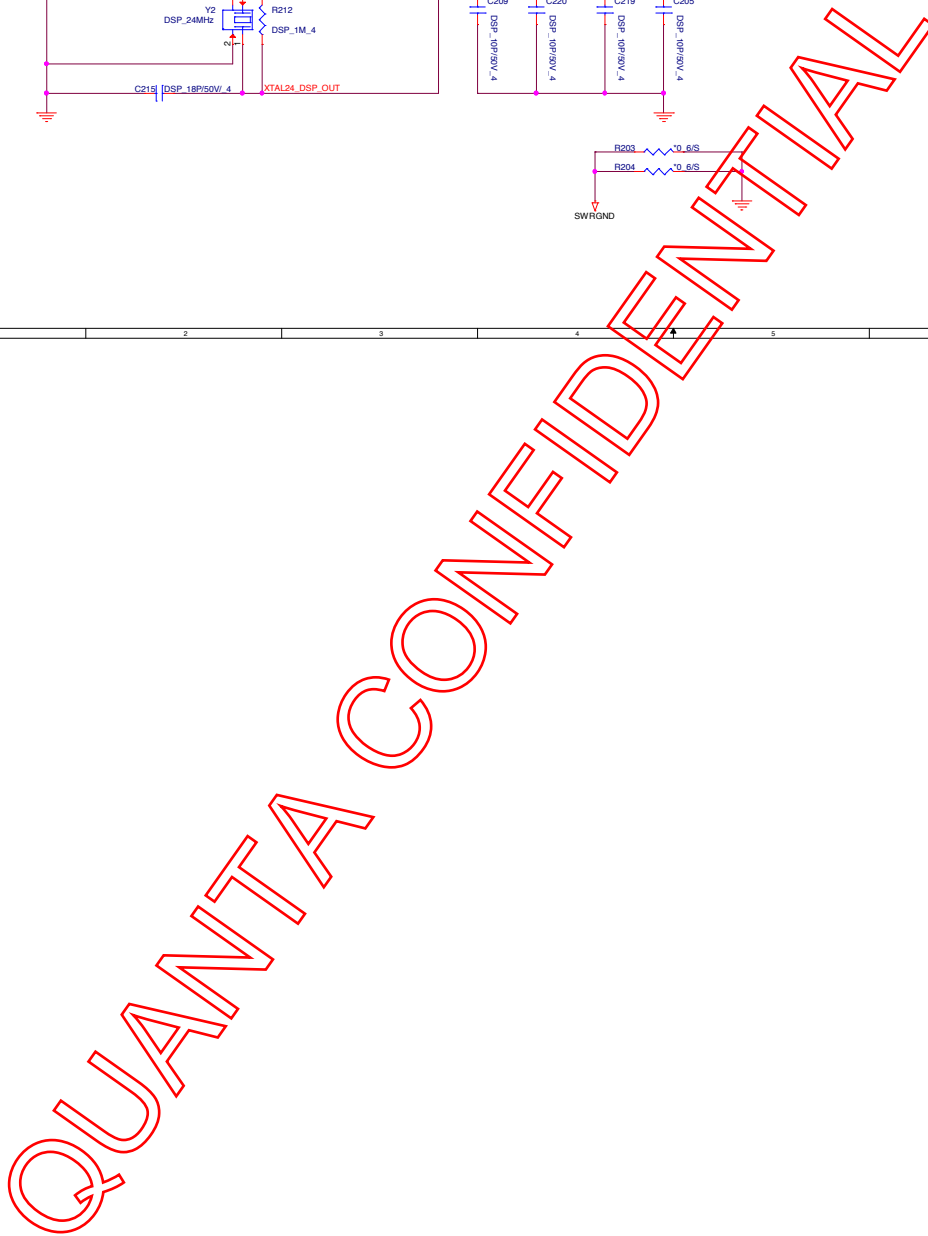


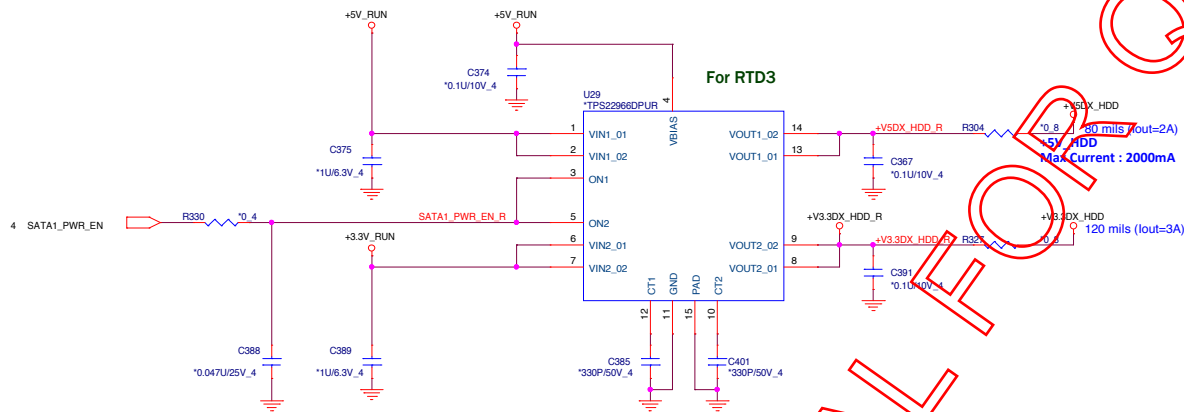
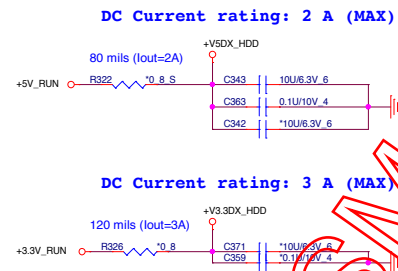
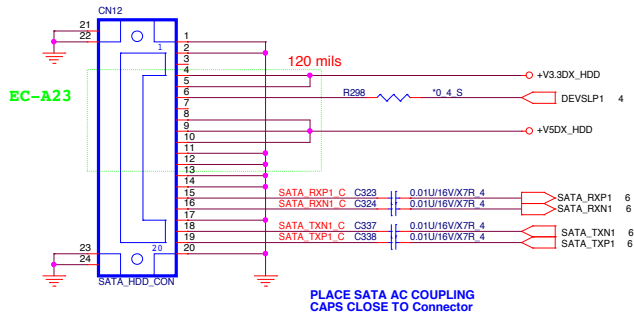
EMI reserve for HDMI



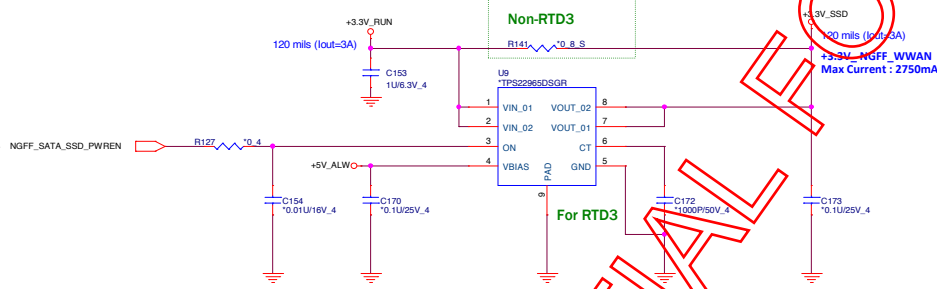
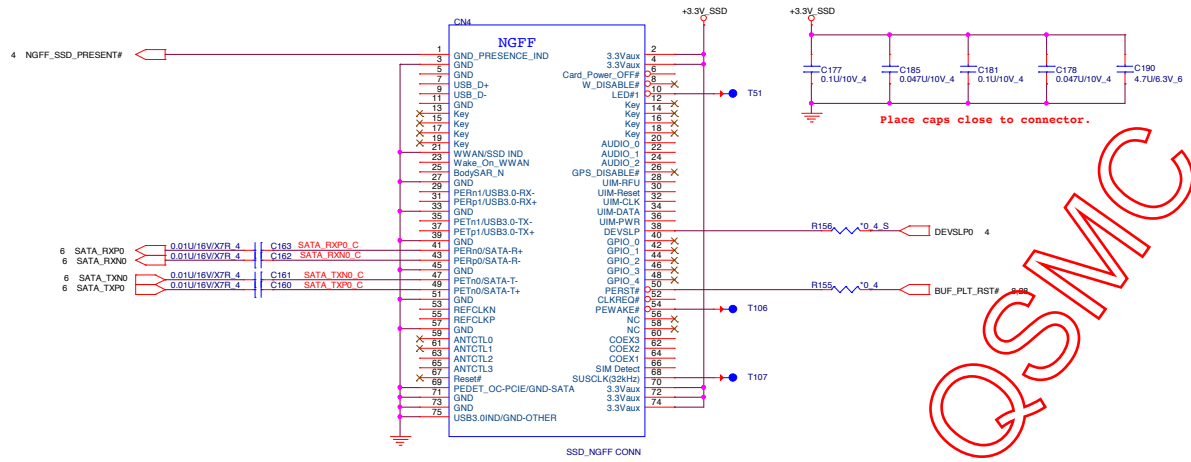
	PROJECT : L29A	
	Quanta Computer Inc.	
Size	Document Number	Rev
	HDMI CONN	1A
Date:	Monday, April 15, 2013	Sheet 22 of 47



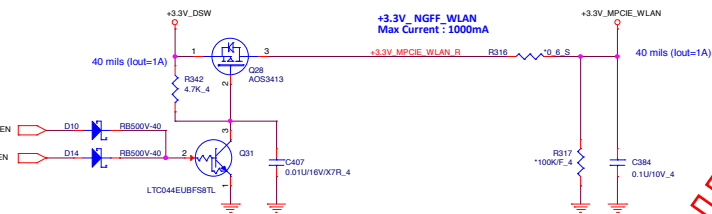


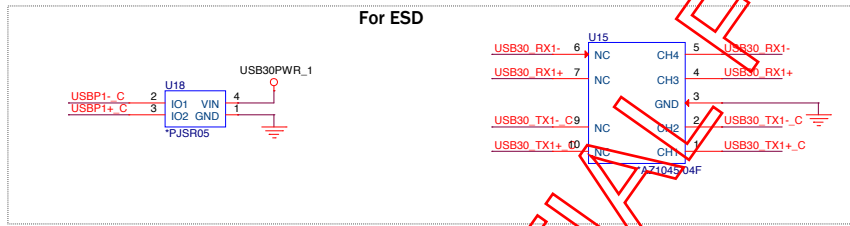
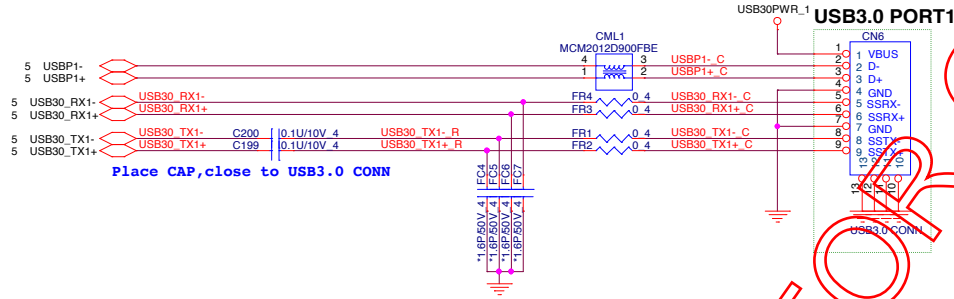
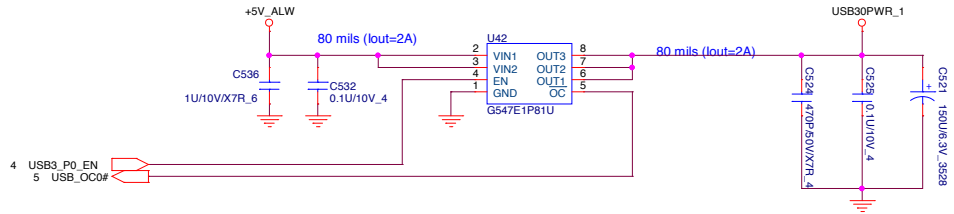


NGFF SSD connector



28

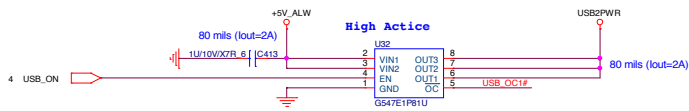




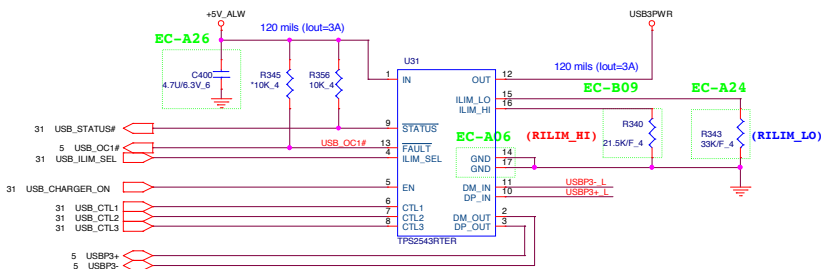
PROJECT : LZ9A
Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x1	1A
Date:	Monday, April 15, 2013	Sheet 29 of 47

USB 2.0 Port



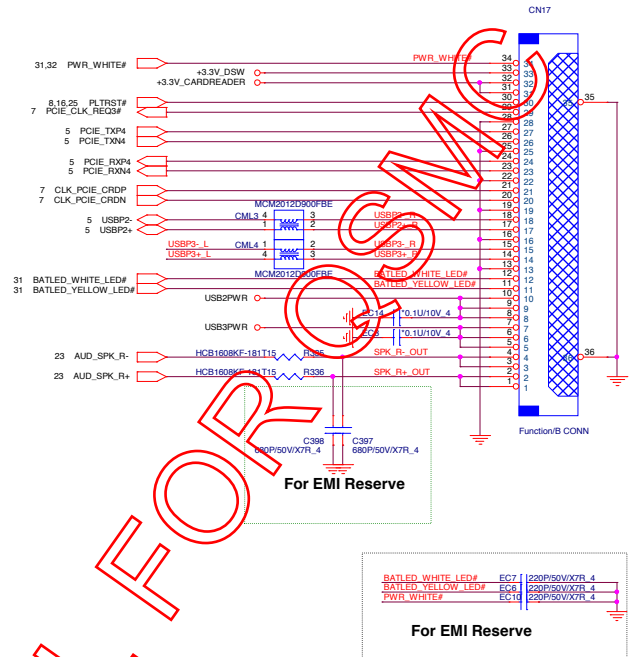
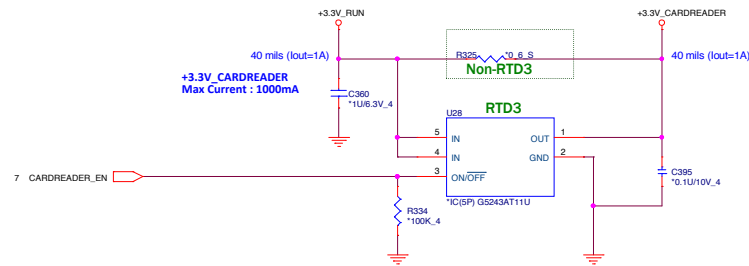
USB Charger 2.0 Port

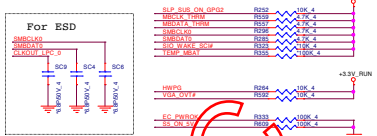


RILIM LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
 1. ILIM_SEL is always set high
 2. Load Detection - Port Power Management is not used
 3. Mouse / keyboard wake function is not used
 If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM LO < 80.6 kΩ.
 The following equation programs the typical current limit:
 (1) RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

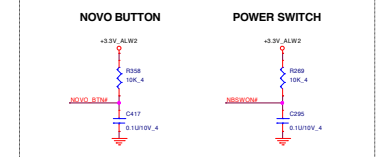
$$I_{OS_typ}(mA) = \frac{50,500}{(R_{ILIM_XX}(k\Omega) + 0.1)}$$


Card Reader VCC Control





Note:
 1. IT8567 with 128K-byte e-flash
 Auto load code condition:
 1. Let PCH SPI interface in High-Z state.
 2. RSMRST# pull low
 (PCH SPI pins are tri-stated prior to RSMRST# de-assertion)
 3. EC pin 100(GPG2) pull high(force EC load code)
 4. Supply power to SPI flash ROM, PCH(VCCSPI, +1.05V_SUS) and EC



	PROJECT : LZ9A Quanta Computer Inc.		
	Size Custom	Document Number KBC IT8587	Rev 1A
Date: Monday, April 15, 2013		Sheet 31 of 47	

KEYBOARD

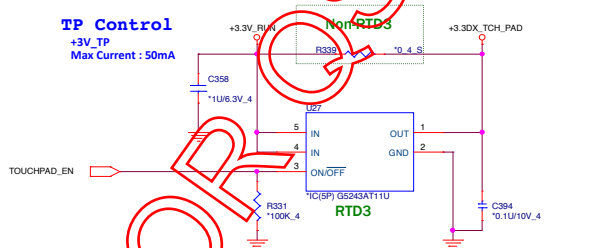
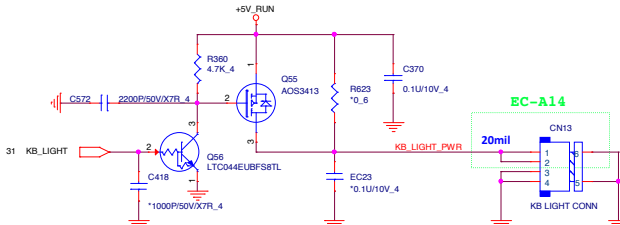
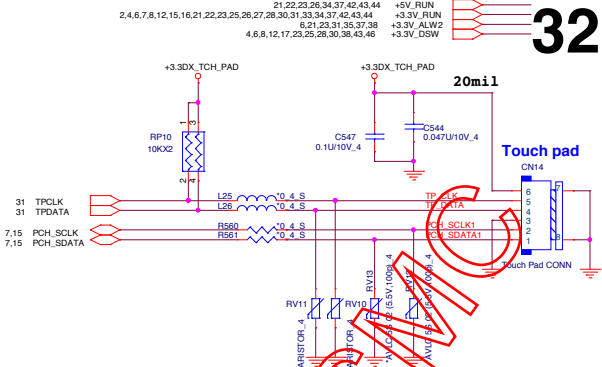
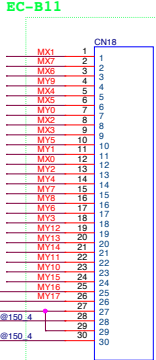
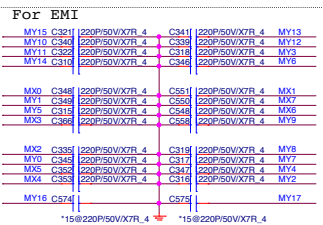
Pinout diagram for the MX150-2601-3 keyboard connector. The diagram shows a 26-pin connector with pins numbered 1 to 26. Pins 1 through 15 are labeled with MX1 through MX15. Pins 16 through 26 are labeled with MX16 through MX26. The connector is shown with a blue ribbon cable. The diagram is labeled 'KEYBOARD' at the top and 'CN15' at the bottom right. The pin numbers are listed on the left side of the connector.

Pin Number	Label
1	MX1
2	MX2
3	MX3
4	MX4
5	MX5
6	MX6
7	MX7
8	MX8
9	MX9
10	MX10
11	MX11
12	MX12
13	MX13
14	MX14
15	MX15
16	MX16
17	MX17
18	MX18
19	MX19
20	MX20
21	MX21
22	MX22
23	MX23
24	MX24
25	MX25
26	MX26

3+3V_{CC} RUN **QTD** R324 150.4

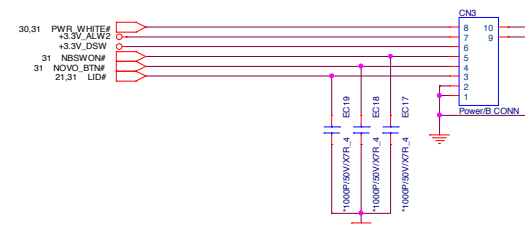
CN15

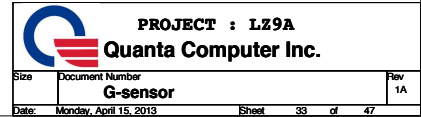
196153-26041-3

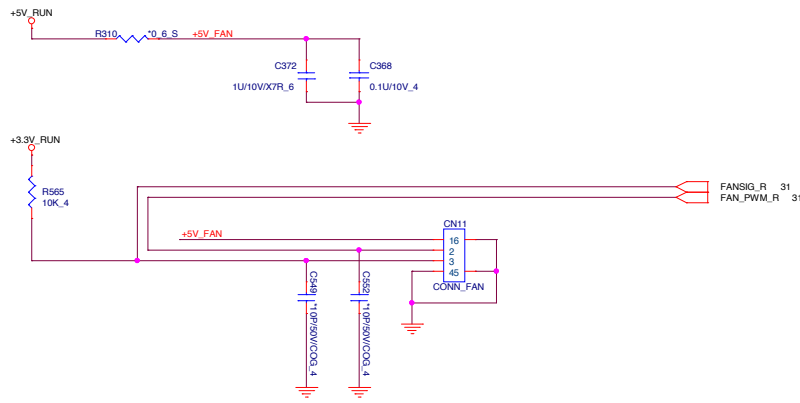


Power Board CONN

The diagram illustrates the power board connection. On the left, a connector labeled '30,31' is shown with five pins. The top two pins are labeled 'PWR_WHITE' and '+3.3V_ALW2'. The bottom three pins are labeled 'NBSWONF', 'NOVO_STMF', and '21,31_LIDF'. These pins are connected to the 'CNS' module on the right. The 'CNS' module has pins 1 through 10. Pin 1 is connected to ground. Pin 2 is connected to the '21,31_LIDF' pin. Pin 3 is connected to the 'NOVO_STMF' pin. Pin 4 is connected to the 'NBSWONF' pin. Pin 5 is connected to the '+3.3V_ALW2' pin. Pin 6 is connected to the 'PWR_WHITE' pin. Pin 7 is connected to ground. Pin 8 is connected to ground. Pin 9 is connected to ground. Pin 10 is connected to ground. The 'CNS' module is labeled 'Power/B CONN'. Below the 'CNS' module, three capacitors are shown: 'EC19' (100pF/50V/X7R_4), 'EC18' (100pF/50V/X7R_4), and 'EC17' (100pF/50V/X7R_4). Each capacitor is connected to ground and to the power lines from the 'CNS' module.

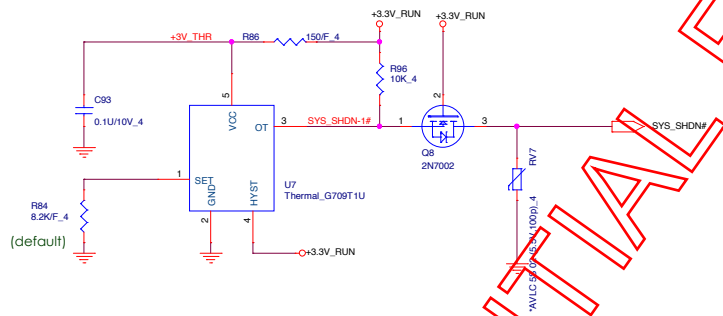







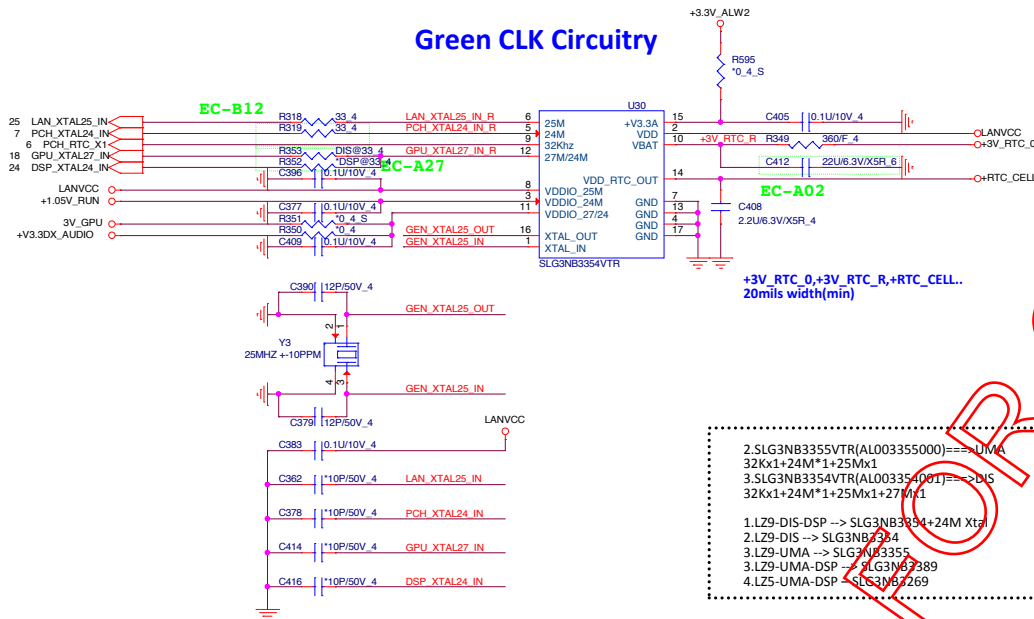
QUANTA CONFIDENTIAL FOR QSMC

Thermal Sensor

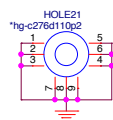
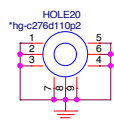
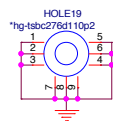
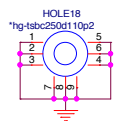
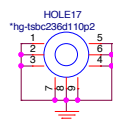
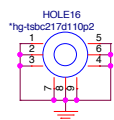
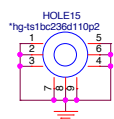


 PROJECT : LZ9A Quanta Computer Inc.		
Size	Document Number	Rev
	FAN/Thermal	1A
Date:	Monday, April 15, 2013	Sheet 34 of 47

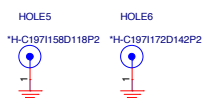
Green CLK Circuitry



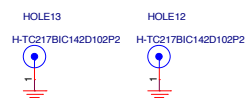
- 2.SLG3NB3355VTR(AL003355000)===>UMA 32Kx1+24M*1+25Mx1
- 3.SLG3NB3354VTR(AL003354001)===>DIS 32Kx1+24M*1+25Mx1+27Mx1
- 1.LZ9-DIS-DSP --> SLG3NB3354+24M Xta
- 2.LZ9-DIS --> SLG3NB3354
- 3.LZ9-UMA --> SLG3NB3355
- 3.LZ9-UMA-DSP --> SLG3NB3389
- 4.LZ5-UMA-DSP --> SLG3NB3269



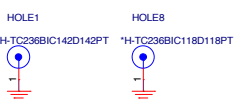
CPU HOLE



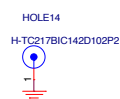
WLAN HOLE



VGA HOLE



SSD HOLE



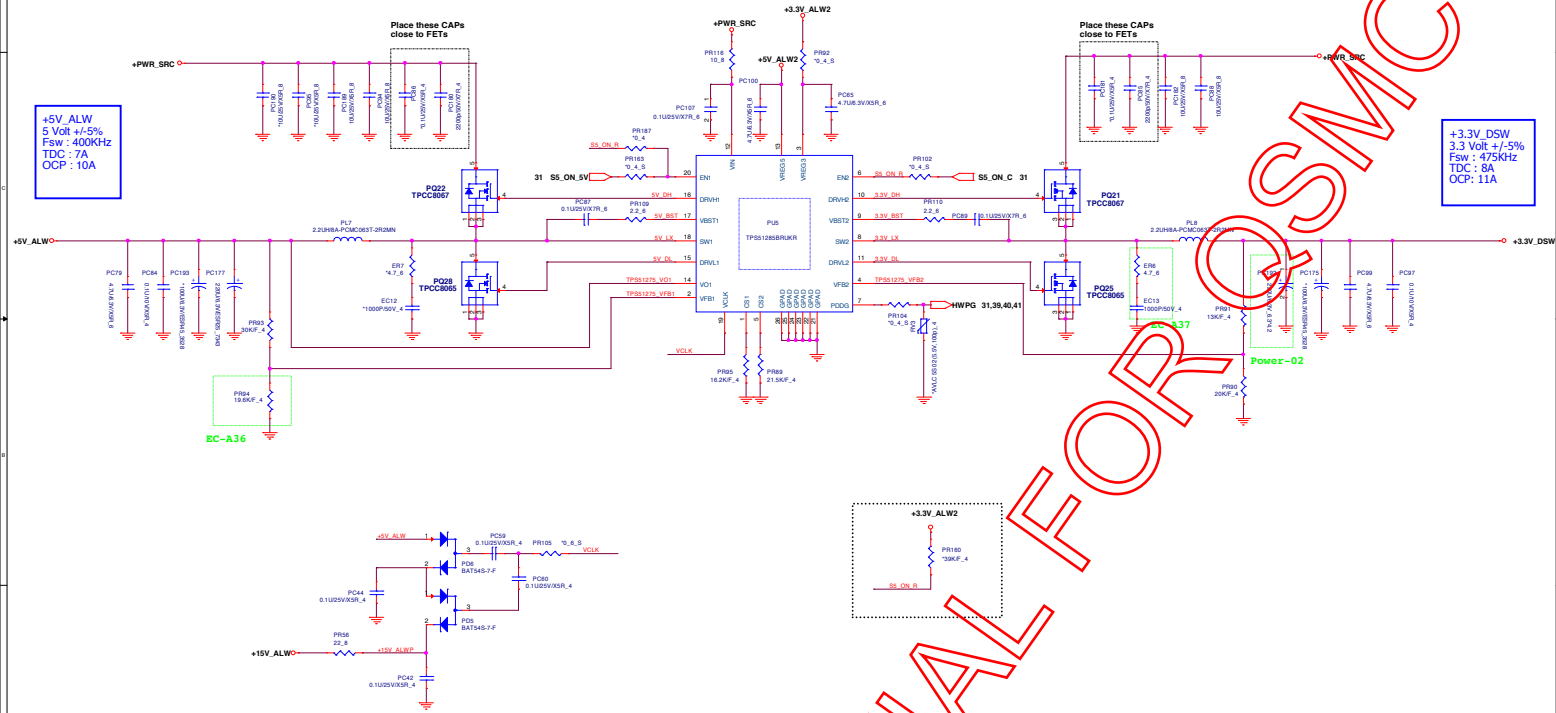
ESD

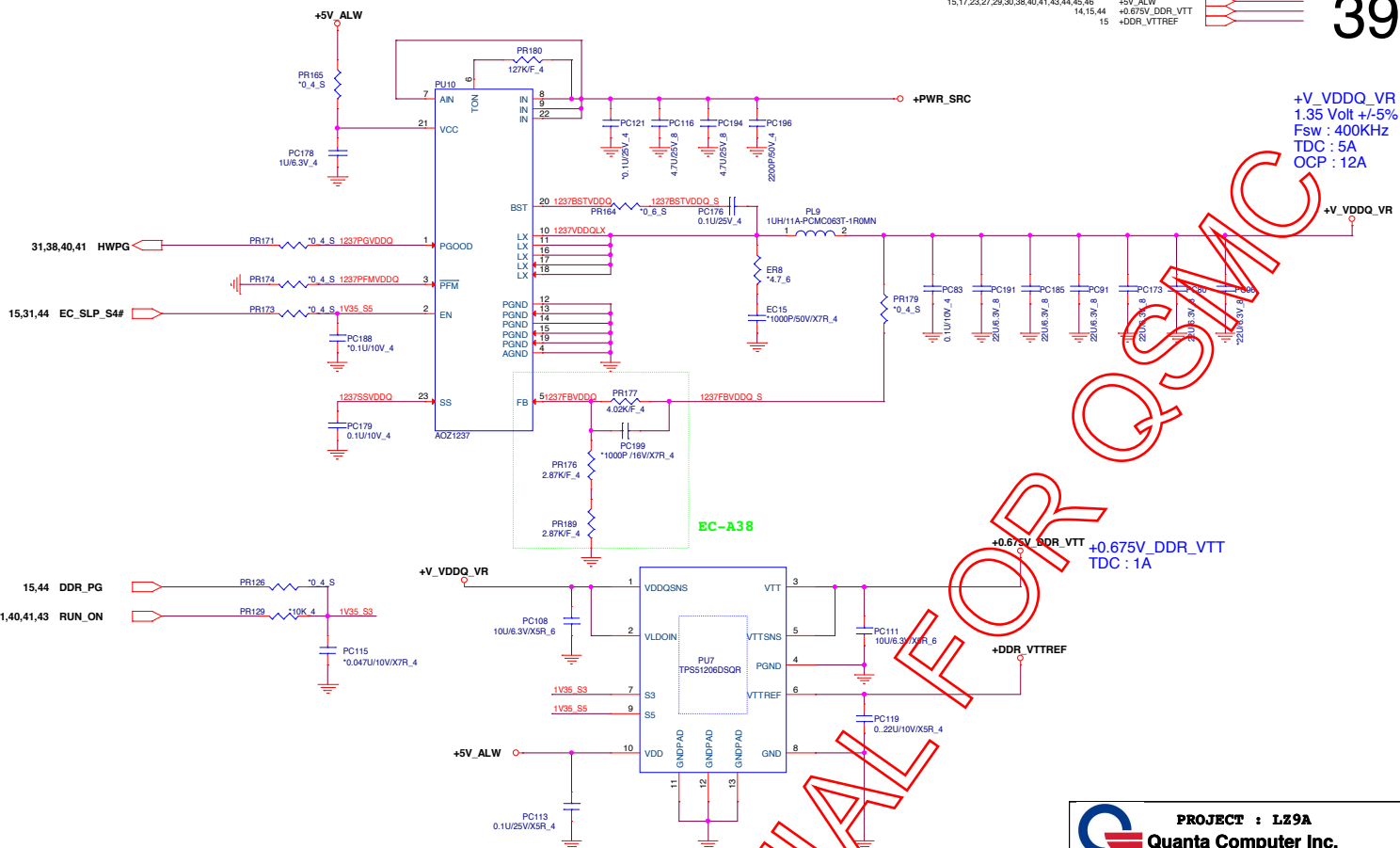


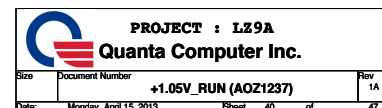
PROJECT : LZ9A
Quanta Computer Inc.

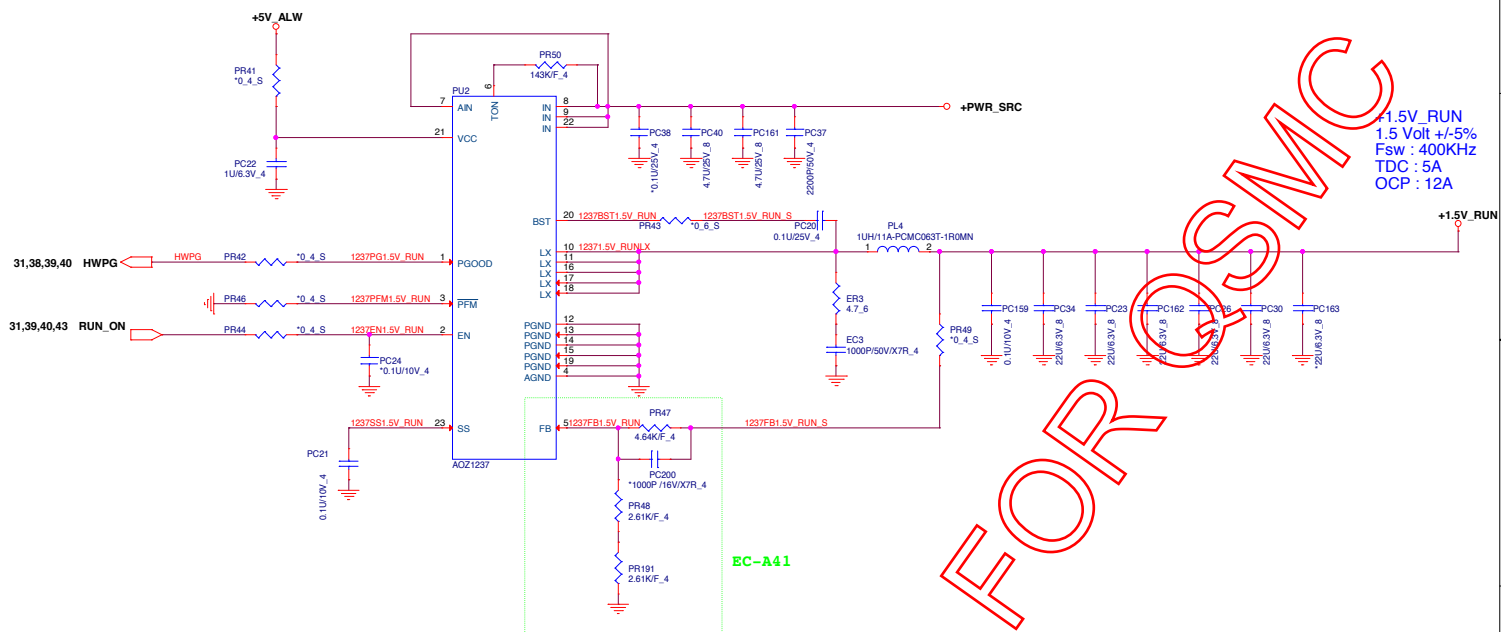
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date:	Monday, April 15, 2013	Sheet 36 of 47




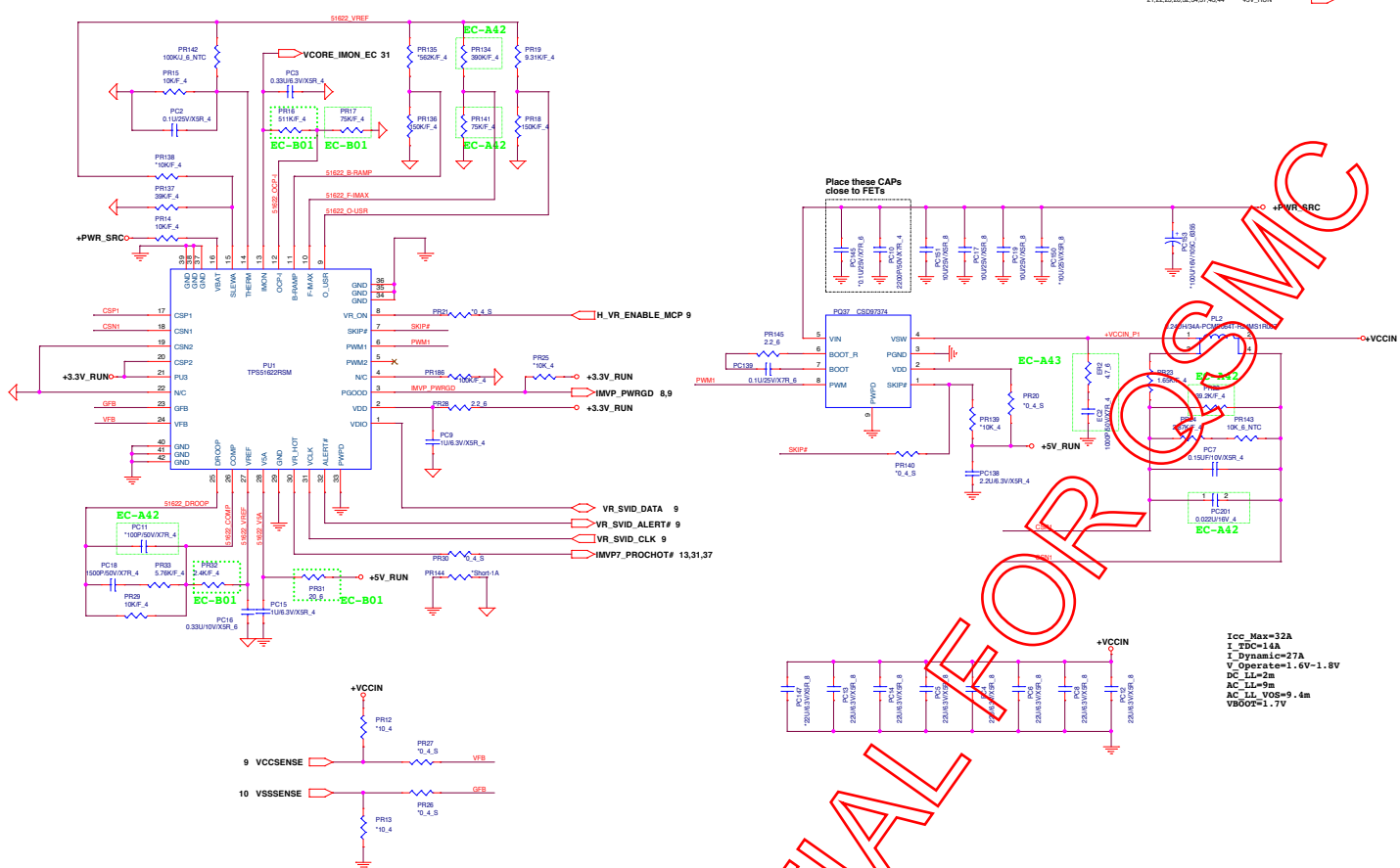




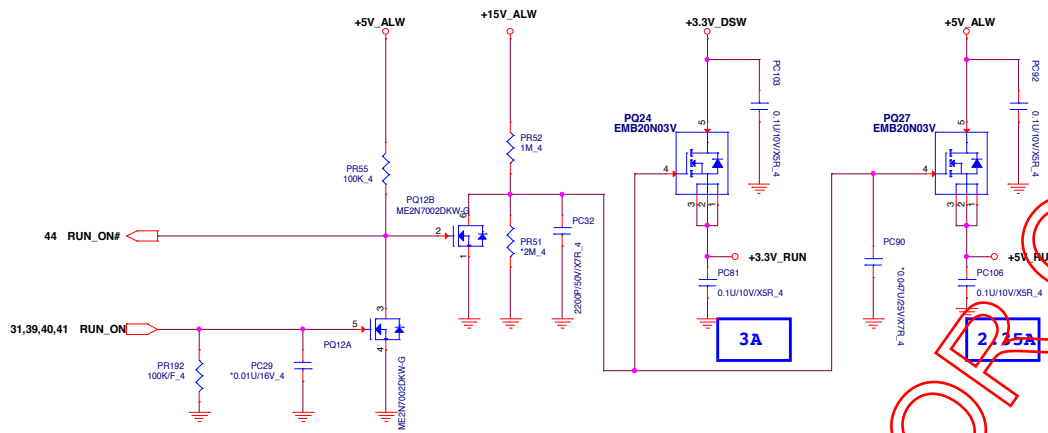





 PROJECT : L29A Quanta Computer Inc.			
Size	Document Number	+1.5V_RUN (AOZ1237)	
Date	Monday, April 15, 2013	Sheet	41 of 47

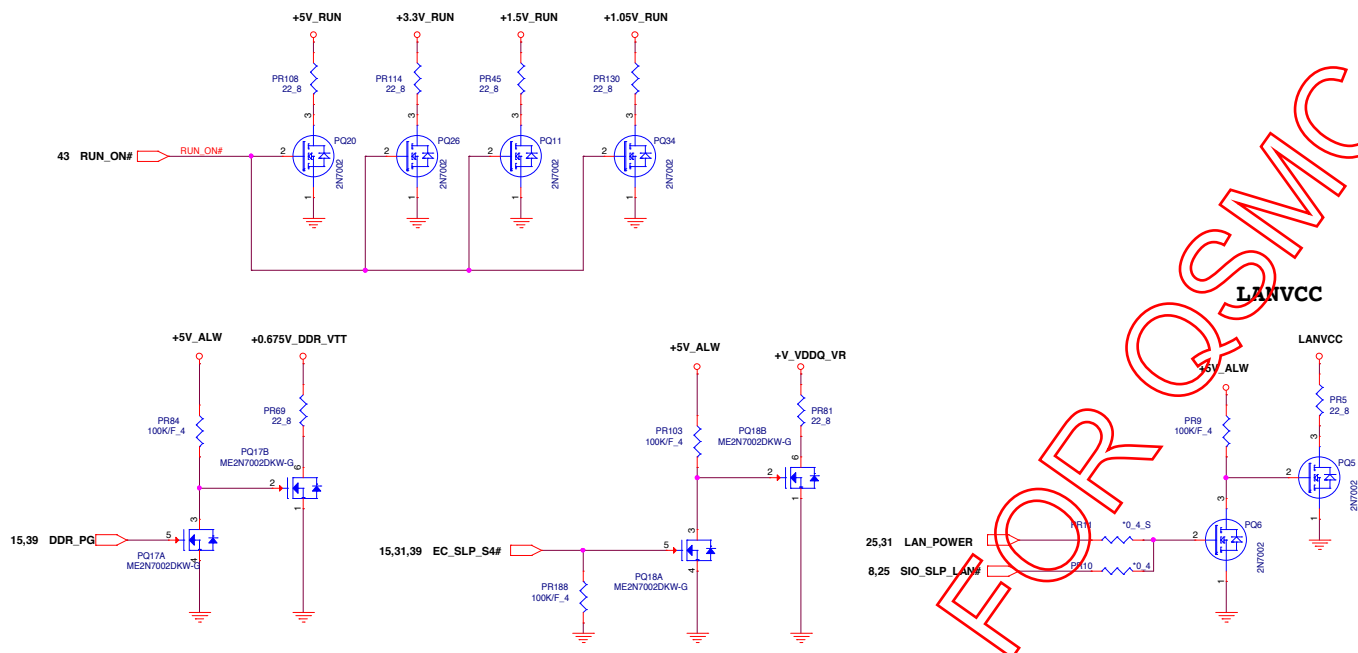
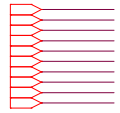



```
Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V-1.8V
DC_LL=2m
AC_LL=9m
AC_LL VOS=9.4m
VBOOT=1.7V
```

	PROJECT : LZ9A		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	Load Switch	1A	
Date:	Monday, April 15, 2013	Sheet	43 of 47

15,17,23,27,29,30,38,39,40,41,43,45,46
21,22,23,26,32,34,37,42,43
2,4,6,7,8,12,15,16,21,22,23,25,26,27,28,30,31,32,33,34,37,42,43
+5V_ALW
+5V_RUN
+3.3V_RUN
+1.5V_RUN
+1.05V_RUN
+0.675V_DDR_VTT
+3.3V_DEEP_SUS
+V_VDDQ_VR
LANVCC
+15V_ALW



**PROJECT : L29A**
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	
Date: Monday, April 15, 2013	Sheet 44 of 47	1

QUANTA CONFIDENTIAL

